CLAIMS

What is claimed is:

1. A semiconductor design for easing detection of out-of-focus conditions during lithographic processing, the design patternable on a semiconductor wafer and comprising:

a central main body; and

an arm extending from a side of the central main body having a first one or more at least substantially triangular shapes and a disconnected second one or more at least substantially triangular shapes, a tip of the first one or more at least substantially triangular shapes positioned opposite a tip of the second one or more at least substantially triangular shapes, such that a gap there between is formed.

2. The design of claim 1, wherein the central main body is at least substantially rectangular in shape.

3. The design of claim 1, wherein the arm extends from the side of the central main body less than half-way down from a top of the central main body.

4. The design of claim 1, wherein each of the first and the second one or more at least substantially triangular shapes comprises one or more triangles.

5. The design of claim 4, wherein the one or more triangles comprise a single triangle.

6. The design of claim 1, further comprising a second arm extending from an opposite second side the central main body having a third one or more at least substantially triangular shapes and a disconnected fourth one or more at least substantially triangular shapes, a tip of the third one or more at least substantially triangular shapes positioned opposite a tip of the fourth one or more at least substantially triangular shapes, such that a second gap there between is formed.

7. The design of claim 6, wherein the second arm extends from the opposite side of the central main body less than half-way down from a top of the central main body.

8. The design of claim 6, wherein each of the third and the fourth one or more at least substantially triangular shapes comprises one or more triangles.

9. The design of claim 8, wherein the one or more triangles comprise a single triangle.

10. The design of claim 1, wherein the gap is sensitive to out-of-focus conditions during the lithographic processing.

11. The design of claim 1, wherein the gap increases as defocus increases.

12. The design of claim 11, wherein increasing of the gap as defocus increases is automatically detectable by semiconductor test equipment.

13. A method for detecting out-of-focus conditions during lithographic processing comprising:

automatically measuring at a focus setting a gap formed within a semiconductor design patterned on a semiconductor wafer, the semiconductor design having a central main body and at least one arm extending from sides of the central main body, each arm having a first one or more at least substantially triangular shapes and a disconnected second one or more at least substantially triangular shapes, a tip of the first one or more at least substantially triangular shapes positioned opposite a tip of the second one or more at least substantially triangular shapes, the gap formed there between;

comparing the gap against a specification; and

concluding that defocus has resulted where the gap is out of the specification.

14. The method of claim 13, further initially comprising patterning the semiconductor design on the semiconductor wafer.

15. The method of claim 13, further comprising, otherwise concluding that defocus has not resulted where the gap is within the specification.

16. The method of claim 13, further comprising, where the gap is out of the specification:

changing the focusing setting; and

repeating measuring at the focus setting the gap, comparing the gap against the specification, and concluding that defocus has resulted where the gap is out of the specification, until the gap is within the specification.

17. The method of claim 13, wherein the gap is sensitive to out-of-focus conditions during the lithographic processing.

18. The method of claim 13, wherein the gap increases as defocus increases.

19. The method of claim 18, wherein increasing of the gap as defocus increases is automatically detectable by semiconductor test equipment.

20. A system comprising:

a semiconductor test equipment having an automatic mode of defocus detection;

a semiconductor design having a central main body and at least one arm extending from sides of the central main body, each arm having a first one or more at least substantially triangular shapes and a disconnected second one or more at least substantially triangular shapes, a tip of the first one or more at least substantially triangular shapes positioned opposite a tip of the second one or more at least substantially triangular shapes, a gap formed there between; and

a semiconductor wafer on which the semiconductor design is patterned, the gap of the semiconductor design increasing as defocus increases, such that the automatic mode of defocus detection is able to detect when the gap is out of a predetermined specification, for concluding that unacceptable defocus has resulted.